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EXAMINER	
TAKAOKA, DEAN O	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,748	HANGAI ET AL.	
	Examiner	Art Unit	
	DEAN O. TAKAOKA	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "said SPST" in page 4. There is insufficient antecedent basis for this limitation in the claim.

No previous recitation of a “SPST” can be found in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakahara et al. (US 5,485,130) for reasons of record contained in the office action dated November 12, 2008.

Claim 1. Nakahara (Figs. 1, 7 et al.) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (15) and an output terminal (16), said SPST switch comprising: a plurality of field-effect transistor

(FET) switches connected in parallel (7a,b)(parallel connection to transmission line), each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor (direct connection of drain and source to inductor shown and analogous to Applicant's showing), wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch; (it is the position of the Examiner that the connections of the input and outputs of FET switches are in a parallel to transmission line and most similar to Applicant's shunt connections sans Fig. 25 which is a series connection and not parallel); each of said field-effect transistors has an ON state and an OFF state changed by a voltage applied to a gate of each of said field-effect transistors (6a,b), and each of said field-effect transistors has an OFF capacitance that causes parallel resonance with said inductor connected at a frequency of the high frequency signal (col. 1, lns 40-43).

9. An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals (Fig. 1), said SPDT switch employing: a plurality of field-effect transistor (FET) switches connected in parallel (7a,b), each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor, wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the

output terminal of said SPST switch (discussed in the reasons for rejection of claim 1 above).

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunaga et al. (US 4,789,846) for reasons of record contained in the office action dated November 12, 2008.

Claim 1. Matsunaga (Fig. 6 et al.) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (to node 2) and an output terminal (nodes to 3 or 4), said SPST switch comprising: a plurality of field-effect transistor (FET) switches connected in parallel (10, 14, 38)(parallel connection to transmission line), each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor (5, 6, 43)(direct connection of drain and source to inductor shown an analogous to Applicant's showing), wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch (it is the position of the Examiner that the connections of the input and outputs of FET switches are in a parallel to transmission line and most similar to Applicant's shunt connections sans Fig. 25 which is a series connection and not parallel); each of said field-effect transistors has an ON state and an OFF state changed by a voltage applied to a gate of each of said field-effect transistors (shown), and each of said field-effect transistors has

an OFF capacitance that causes parallel resonance with said inductor connected at a frequency of the high frequency signal (col. 8, lns 30-32).

9. An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals (Fig. 6), said SPDT switch employing: a plurality of field-effect transistor (FET) switches connected in parallel (where the signal is branched to 3 or 4), each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor, wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch (discussed in the reasons for rejection of claim 1 above).

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Wallace (US 6,137,377).

Claim 12. Wallace (Fig. 7C et al.) shows an MPMT (multiple-pole multiple throw) switch for controlling propagation of a high frequency signal between a plurality of input terminals (RFinx, RFiny) and a plurality of output terminals (RFoutx, RFouty), said MPMT switch employing: a plurality of field-effect transistor (FET) switches, each of said FET switches having an inductor directly connected in parallel with a series circuit (parallel shunt inductor to series FET), the series circuit consisting. of a capacitor connected in series with a drain or source of a field-effect transistor (series capacitor

shown as 4.5pf).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 – 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumitsu et al. (JP 05-299995) prior art cited in Applicant's IDS of July 21, 2006 in view of Nakahara et al. (US 5,485,130) or Matsunaga et al. (US 4,789,846) for reasons of record contained in the office action dated November 12, 2008.

1. Tokumitsu (Fig. 6) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (25) and an output terminal (26 or 27), said SPST switch comprising: first field-effect transistor switch connected in parallel (4b), which includes a field-effect transistor having its drain and source connected in parallel with an inductor (L2), wherein said field-effect transistor has its ON state and OFF state changed by a voltage applied to a gate of each of said field-effect transistors (14'), and said field-effect transistors has its OFF capacitance cause parallel resonance with said inductor connected at a frequency of the high frequency signal (equation) but does not show a plurality of parallel connected field-

effect transistors each having its drain and source connected in parallel with an inductor.

Nakahara or Matsunaga shows similar SPST switches comprising a plurality of field-effect transistor switches connected in parallel, which includes a plurality of field-effect transistor having its drain and source connected in parallel with an inductor (discussed in the reasons for rejection above).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the switch disclosed by Tokumitsu with the plural FET switches including parallel inductors disclosed by Nakahara et al. or Matsunaga et al. Such a modification would have been obvious where both circuits are drawn to microwave switching; where each specific FET switch including parallel inductor and is resonant; where Nakahara teaches the advantage of maximum allowable value of incident power is increased in an antenna switch circuit (abstract); or where Matsunaga teaches solving the problems of increased manufacturing steps required for increased input power and allowing high voltages for decreased substrate area (col. 5, lns 23-37) thus suggesting the obviousness of the modification.

4. An SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal and an output terminal, said SPST switch comprising: a field-effect transistor (FET) switch constructed by directly connecting an inductor in parallel with a series circuit (where Nakahara, Matsunaga and Tokumitsu all show direct connection of a parallel inductor to the FET), the series circuit consisting of a capacitor connected in series with a drain or source of a FET (where Tokumitsu

shows a series capacitor connection; C1 or C2 – Fig. 6), wherein said FET has an ON state and an OFF state changed by a voltage applied to a gate of said FET, and said FET has a parasitic inductor and said capacitor that cause series resonance, and has an OFF capacitance which causes parallel resonance with said inductor (abstract – Tokumitsu).

5. The SPST switch according to claim 4, wherein the input of said second FET switch is directly connected to the input terminal of said SPST switch and the output of said FET switch is directly connected to the output terminal of said SPST switch (where Nakahara and Matsunaga show parallel direct connections of the FETs to the input and outputs of the transmission line and discussed in the reasons for rejection of the claims above).

6. The SPST switch according to claim 5, further comprising a plurality of second FET switches connected in parallel between the input terminal and the output terminal (Matsunaga – Fig. 6).

7. The SPST switch according to claim 4, wherein the input terminal of said FET switch is directly connected to the input terminal or the output terminal of said SPST; and the output of said FET switch is directly connected to ground (where Nakahara, Matsunaga and Tokumitsu all show direct connections of the FETs to the input and outputs of the transmission line and discussed in the reasons for rejection of the claims above as well as direct connections of the FETs to ground).

8. The SPST switch according to claim 7, further comprising a plurality of FET switches connected in parallel wherein the input of said plurality of parallel FET switches is

directly connected to the input terminal of said SPST and the output of said plurality of parallel FET switches is directly connected to ground (discussed in the reasons for rejection of the claims above).

10. The SPDT switch of claim 9, further comprising: a single field-effect transistor (FET) switch having an inductor directly connected in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of a field-effect transistor; and wherein the input of said single FET switch is directly connected to ground. (parallel connection of the inductor and ground connections discussed in the reasons for rejections above and where Tokumitsu shows a capacitor (C_2) connected in series with a drain or source of the FET – Fig. 6).

Response to Arguments

Applicant's arguments, see pages 7, 8, filed February 27, 2009, with respect to drawing rejections and rejections of claims 4-8, 10 and 12 have been fully considered and are persuasive. The objections/rejections of the drawings and rejection under respective claims has been withdrawn. (Applicant's arguments I. and II.)

Applicant's arguments with respect to rejections under Nakahara et al., Matsunaga et al. or Tokumitsu et al. have been fully considered but they are not persuasive. (Applicant's arguments III and IV.)

Applicant's arguments, with respect to the rejection(s) of claim(s) 12 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection

has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wallace.

III. Claim Rejections Under 35 U.S.C. 102(b)

Applicants submit "*Nakahara discloses a number of different switch circuits. For example, Figure 1 discloses a SPDT switch, however, the field-effect transistors are neither connected in parallel nor connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch. Figure 7 discloses a switch in which two field-effect transistors separated by a transmission line (14). Therefore, Figure 7 fails to disclose parallel field-effect transistors. In addition, Figure 7 fails to disclose field-effect transistors in which the inputs of the field-effect transistors are connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch."* which the Examiner disagrees.

Nakahara shows shunt connected FETs, thus connected in parallel to the input/ouput transmission path. Furthermore, Nakahara shows each FET directly connected to the input and output of the transmission path as illustrated in Fig. 7 (and analogous to Applicants showing of direct connections of FETs). If the Applicant has intended to suggest the **FETs connected in parallel to each other (emphasis added)** (see Applicants Fig. 4 et al.), this is not commensurate with that which is being claimed, thus the rejections are maintained by the Examiner.

Applicants submit "*Matsunaga discloses a number of different semiconductor switches. For example, Figure 6 discloses a SPDT switch, however, the field-effect transistors are neither connected in parallel nor connected directly between the input*

terminal of the SPST switch and the output terminal of the SPST switch. Figures 5(a), 5(b) and 6 disclose FET 14 and FET 38 which are not directly connected in parallel, rather, there is a one quarter wave length between drain 15 of FET 14 and drain 40 of FET 14 (Column 7, lines 46 to 56). Therefore, Matsunaga fails to disclose parallel field-effect transistors. In addition, Matsunaga fails to disclose field-effect transistors connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch." which the Examiner disagrees.

As with Nakahara above, Matsunaga shows shunt connected FETs, thus connected in parallel to the input/ouput transmission path. Furthermore, Matsunaga shows each FET directly connected to the input and output of the transmission path as illustrated in Fig. 7 (and analogous to Applicants showing of direct connections of FETs). While Matsunaga shows a transmission line length (3) (Fig. 6), Applicants showing of direct connection also comprise a length of transmission line to the input and output, inherent where the FETs are not directly connected to input/output terminals, thus Matsunaga also comprising a direct connection. With respect to parallel connections, as with Nakahara above, if the Applicant has intended to suggest the **FETs connected in parallel to each other (emphasis added)** (see Applicants Fig. 4 et al.), this is not commensurate with that which is being claimed, thus the rejections are maintained by the Examiner.

IV. Claim Rejections Under 35 U.S.C. 103(a)

(Claims 1 – 8 and 10)

Applicants submit "*Tokumitsu describes a microwave semiconductor switch that consists of two circuit portions in parallel with each other (Abstract and Figure 1). The first circuit portion consists of a switch in series with an inductor. The second circuit portion consists of a parallel circuit in series with a capacitor, the parallel circuit being a field-effect transistor in parallel with an indictor (Abstract and Figure 1). Therefore, Tokumitsu fails to disclose a SPST switch "between an input terminal and an output terminal, said SPST switch" constructed by "directly connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of a FET" (Claim 4).*" which the Examiner disagrees.

Tokumitsu (Fig. 6 et al.) clearly shows the SPST switches (SW1-4) between the input terminal (25) and output terminals (26, 27). Furthermore, FETs 1b and 4b each an inductor connected in parallel to the respective FET where limits of the series circuit is not defined thus where both C1 and C2 are series connected to each FET which is analogous to Applicants showing in Fig. 13. As with Nakahara and Matsunaga above, Tokumitsu shows SW1 directly connected to the input (25) and SW2 directly connected to output (27) with corresponding parallel connected inductors.

Applicants further submit "*Figure 6 of Tokumitsu discloses a SPDT switch. The SPDT switch of Tokumitsu has a parallel circuit in series with a capacitor, the parallel circuit being a gate in parallel with an inductor. Additionally, the parallel circuit in series with a capacitor is a first portion of a switch, which is in parallel with a second portion of a switch consisting of a gate in series with an inductor. Tokumitsu fails to disclose a SPST switch comprising a "plurality of field-effect transistor (FET) switches connected in*

parallel, each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor, wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch" (claim 1). Claim 10 is allowable for similar reasons" which the Examiner disagrees.

Tokumitsu (Fig. 6 et al.) clearly shows the SPST switches (SW1-4) which are analogous to Applicants showing where all switches individually are SPST as is well-known in the art. None comprise SPDT which is suggested by the Applicant. Moreover, the shunt connected FETs (SW1, SW 4 – Fig. 6) of Tokumitsu are analogous to Applicants shunt connection such as shown in Figs. 4-9 and 16-24 thus also comprising individual SPST switches. The Examiner invites the Applicant to specifically and distinctly show where in the specification Applicants switches would differ from that shown by Tokumitsu. It is the position of the Examiner that a mere generic recitation of SPST switch does not distinguish over the prior art.

The plurality of parallel connected FETs further comprising inductors connected in parallel to the drain and source are shown by Nakahara or Matsunaga. The direct connection to the input and output of each prior art reference has been discussed above.

Applicants submit "*Nakahara or Matsunaga do not remedy the noted deficiencies of Tokumitsu. This reliance on Nakahara or Matstmaga fails to make up for the deficiencies of Tokumitsu discussed above with respect to independent claims 1 and 4.*

Therefore, the asserted combination of Tokumitsu and Nakahara or Matsunaga (assuming these references may be combined, which Applicants do not concede) fails to establish prima facie obviousness of any pending claim." which the Examiner disagrees.

Tokumitsu, Nakahara and Matsunaga all show nearly identical branched switch devices comprising shunt connected FETs with parallel inductors connected to the drain or source. Furthermore, Tokumitsu shows plural connected FETs where only one FET for each branch is shunt connected. Nakahara and Matsunaga shows plural parallel connected FETs for a branch. Since all references comprise nearly identical branched switch circuits, further comprising nearly identical FET switches with parallel inductors connected to the drain or sources, it is the position of the Examiner that it would have been obvious to combine the references for the reasons of record above and that a *prima facie* case has been made by the Examiner, thus the rejections of record are maintained by the Examiner.

(Claim 11)

Claim 11 has been amended and the rejections under 35 U.S.C. 103(a) have been withdrawn by the Examiner however the amendment contains the limitation "**said SPST**" where only a MPMT (multi-pole multi-throw) switch may be found thus there is insufficient antecedent basis in the claim and is now rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner notes claim 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

(Claim 12)

Claim 12 (previously dependent from claim 4 and now an independent claim) has been amended and the rejections under 35 U.S.C. 103(a) have been withdrawn by the Examiner however a new rejection under 35 U.S.C. 102(b) has been made above as necessitated by amendment.

Allowable Subject Matter

Claim 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: Wallace shows an MPMT (multiple-pole multiple throw) switch for controlling propagation of a high frequency signal between a plurality of input terminals (RFinx, RFiny) and a plurality of output terminals (RFoutx, RFouty), said MPMT switch but does not teach or suggest a plurality of field-effect transistor (FET) switches connected in parallel where the FETs of Wallace are series connected nor would it have been obvious to combine the prior art of record.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN O. TAKAOKA whose telephone number is (571)272-1772. The examiner can normally be reached on 9:00a - 5:30p Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean O Takaoka/
Primary Examiner, Art Unit 2817